R09

Code No: D109115503

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Regular Examinations March 2010
VLSI TECHNOLOGY AND DESIGN
(Common to Embedded Systems, Digital Systems & Computer Electronics, Digital Electronics & Communication Systems, VLSI System Design / VLSI / VLSI Design, Embedded Systems & VLSI Design, VLSI& Embedded Systems, Electronics & Communication Engineering, Systems & Signal Processing)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
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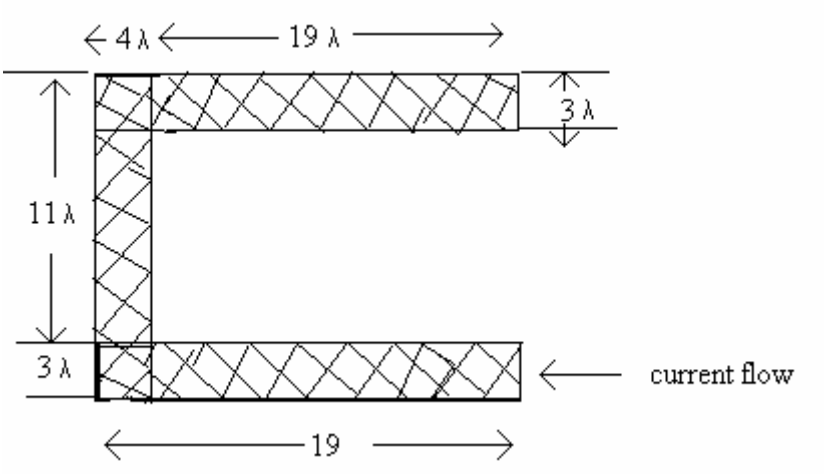
1. a) Explain the fabrication procedure for P-Well CMOS technology.
   b) What are the differences between CMOS and BiCMOS technologies in fabrication?

2. a) Explain how to estimate propagation delay?
   b) Calculate the resistance of the polysilicon wire shown in figure. This polysilicon wire is to be fabricated with a 1μm technology. ($R_s = 4\Omega$/sq).

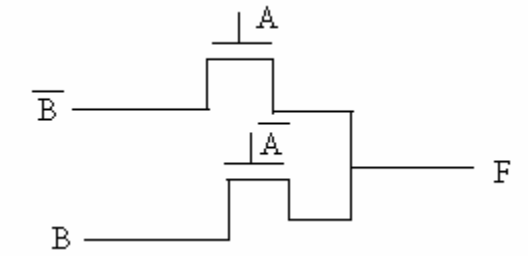


   c) Determine Z_{pu} /Z_{pd} for NMOS inverter driven by another inverter.

3. a) Design a symbolic layout for a complementary CMOS circuit that implements $F= \overline{A + BC}$.
   b) What are the various properties of transmission gate logic?

4. a) What are various limitations of scaling?
   b) What is via? Why these are required in circuit design.

5. Consider the circuit shown in figure.
   i) Determine the logic function F.
   ii) Design a circuit to implement the same logic function using NOR gates.
   iii) Draw a transistor level schematic and use CMOS technology.



6. a) What is clock skew? How it is calculated?
   b) Explain how to optimize power for sequential circuits?

7. Explain Floor-Planning methods for a chip in detail.

8. Write short notes on
   a) Resistive and inductive interconnect delay.
   b) High level Synthesis.

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